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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,648	12/13/2000	Chakravarthy Kosaraju	042390.P10139	2276
7	590 07/07/2003			
Thomas S. Ferrill			EXAMINER	
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 7th Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026		VU, TRISHA U		
		ART UNIT	PAPER NUMBER	
2001		•	2189	
			DATE MAILED: 07/07/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

	•	Application No.	Applicant(s)				
	Office Action Summary	09/737,648	KOSARAJU, CHAKRAVARTHY				
	Simos Motion Summary	Examiner	Art Unit				
	The MAILING DATE of this	Trisha U. Vu	2189				
	The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	e correspondence address				
	A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed.						
	If the period for reply specified above is less than thirty (30) days, a reply lif NO period for reply is specified above, the maximum statutory period with Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	within the statutory minimum of thirty (30) dill apply and will expire SIX (6) MONTHS fro	ays will be considered timely.				
	20) The distribution of the difference of the di						
	2a) This action is FINAL . 2b) This	s action is non-final.					
	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
	4)⊠ Claim(s) <u>1-15</u> is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
	5) Claim(s) is/are allowed.						
	6) Claim(s) is/are rejected.						
	7) Claim(s) is/are objected to.						
	8) Claim(s) are subject to restriction and/or election requirement						
	Application Papers						
	9) The specification is objected to by the Examiner.						
1	10)⊠ The drawing(s) filed on <u>26 March 2001</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
	If approved corrected described on is	: a) ☐ approved b) ☐ disappro	ved by the Examiner.				
	in approved, corrected drawings are required in reply to this Office action						
12) The oath or declaration is objected to by the Examiner.							
1	riority under 35 U.S.C. §§ 119 and 120						
	13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
	a) All b) Some * c) None of:						
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No						
	3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
	14)☐ Acknowledgment is made of a claim for domestic or	iority under 25 LLS O S 4404	l. 				
	14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application). a) The translation of the foreign language provisional application has been received.						
	15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)							
1)	Notice of References Cited (PTO-892)	4) Interview Summary (PTO-413) Paper No(s)				
4) L 3) [Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal Pa	tent Application (PTO-152)				
.S. Pa	Itent and Trademark Office	6)	,				
·TO-	326 (Rev. 04-01) Office Action S	Summary	art of Paper No. 4				

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DETAILED ACTION

1. Claims 1-15 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the group" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-8 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (6,535,939) (hereinafter Arimilli).

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As to claim 1, Arimilli teaches a method comprising: manufacturing a processor having a flexible architecture to service multiple processor platforms (multi-processor topology) as well as different application platforms (to serve variety number of external devices, processors, and/or network) (col. 5, lines 12-26, 55-67, and col. 6, lines 1-6).

As to claim 2, Arimilli further teaches manufacturing the processor to communicate with a device through a point to point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 3, Arimilli further teaches manufacturing an arbiter (bus allocation unit) to alter one or more signal pathways that a signal may travel within the processor (col. 6, lines 58-67 and col. 7, lines 1-10), the arbiter can alter the signal pathways without physically changing the flexible architecture inside the processor (only powering/allocation of wires at the chip changes) (col. 9, lines 31-67).

As to claim 4, Arimilli teaches an apparatus comprising: an arbiter (switch 401/bus allocation unit) (col. 10, lines 33-46) lined to a first processor (processor chip 201) having a flexible architecture; a point to point bus (e.g. buses 208); and a device (device 202c), the first processor connected to the device through the point to point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 5, Arimilli further teaches the arbiter is internal to the processor (col. 10, lines 42-46 and Fig. 2B).

As to claim 6, Arimilli further teaches the arbiter is external to the first processor (col. 10, lines 40-42).

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As to claim 7, Arimilli further teaches the arbiter comprises a component to change a number of ports linked between the first processor and the device without changing the flexible architecture within the processor (col. 9, lines 31-46).

As to claim 8, Arimilli further teaches the device is selected from a group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor (memory, SMPs, or other component) (col. 4, lines 3-12).

As to claim 10, Arimilli further teaches the arbiter comprises a first component and a second component, the first component (part of the switch) to determine a bandwidth between the device and the processor (monitoring the bus usage on the system) (col. 10, lines 63-67), the second component (part of the switch) to provide a control signal to one or more signal pathway switching devices, the control signal to be based upon the bandwidth determination of the first component (the switch system allocates the available configurable buses based on the change in workload and the priority of the components) (note col. 11, lines 1-11 and also col. 7, lines 1-10 wherein a mode bit may be used to tell the processor how the ports are configured).

As to claim 11, Arimilli teaches a method comprising: communicating between a processor (processor chip 201) and a device (device 202c) through a point to point bus Fig. 1B); using a signal pathway internal to the processor during the communications between the processor and the device; and changing the signal pathway within the processor to optimize a connection for an application (by the switch logic) (col. 10, lines 37-67 and col. 11, lines 1-11).

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As to claim 12, Arimilli further teaches to optimize a connection comprises altering the bandwidth between a first processor and a device exterior to the first processor (col. 11, lines 1-11).

As to claim 13, Arimilli further teaches to optimize a connection comprises altering a number of processors connected to the device (col. 9, lines 36-46).

As to claim 14, Arimilli further teaches the application is selected from a group consisting of a work station application, a server application, a two processor platform, a four processor platform, or an eight processor platform (to serve variety number of external devices, processors, and/or network) (col. 5, lines 12-26, 55-67, and col. 11, lines 49-52).

As to claim 15, Arimilli further teaches the changing of the signal pathway consists of changing a setting in a configuration register (register(s) that hold the setting of the buses) to direct an arbiter to send a control signal to one or more signal pathway switching devices located in the processor (col. 7, lines 2-10, lines 56-64, and col. 8, lines 25-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (6,535,939) (hereinafter Arimilli) as applied to claim 4 above, and further in view of Walker (6,321,269).

As to claim 9, Arimilli does not explicitly disclose the processor comprises a protocol layer; an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer. Walker teaches an information transfer layer (physical layer); a buffer layer (link layer); and a protocol layer (other upper layer(s) of the client/server to further process the data); wherein the information transfer layer is to electronically transfer information on a physical medium between the protocol layer and a device; the buffer layer is to buffer an electronic transfer of information between the protocol layer and the information transfer layer (Fig. 2 and col. 3, lines 49-67, and col. 4, lines 1-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an information transfer layer, a buffer layer, and a protocol layer as taught by Walker in the system of Arimilli to expand communication to a network.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Trisha U. Vu Examiner Art Unit 2189

uv June 25, 2003

> Glenn Å. Auve Primary Patent Examiner Technology Center 2100